ICS 233: Computer Architecture & Assembly Language
Fall Semester 2021 (211) – Section 01
Quiz 5

Name: *ID#*

Q1. Consider the single-cycle datapath and control given at the back of the paper along with the ALU and PC Control logic design for the MIPS processor implementing a subset of the instruction set

a. (4 points) Show the control signals generated for the execution of the following instructions by filling the table given below:

Control Signals									
Op	**RegDst**	**RegWr**	**ExtOp**	**ALUSrc**	**MemRd**	**MemWr**	**WBdata**	**ALUOp**	**PCSrc**
addu	1	1	x	0	0	0	0	ADD	0
lw	0	1	1	1	1	0	1	ADD	0

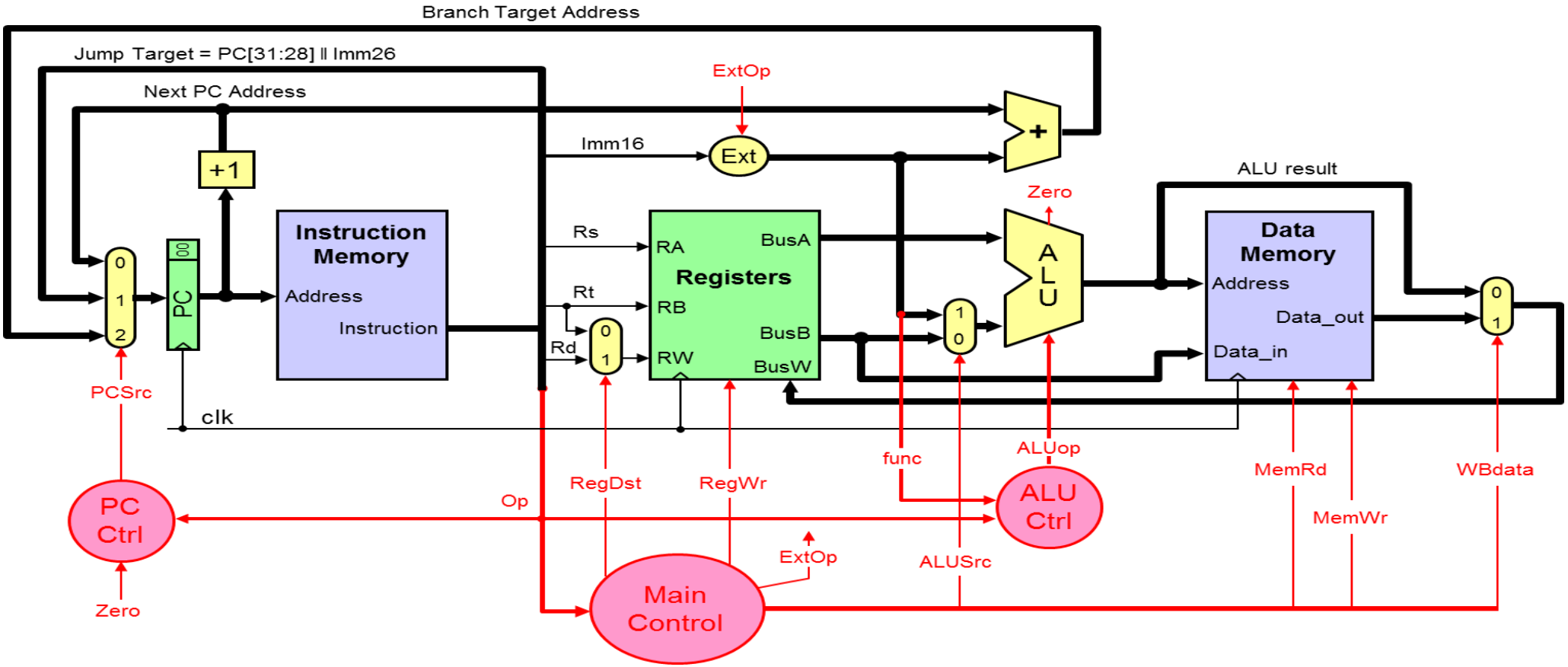
b. (6 points) We want to add the following instructions to the MIPS single-cycle datapath. Made any necessary modifications to the datapath, ALU or PC control block and the control signals needed for the implementation of these instructions. If no modifications to the datapath are required for implementing a given instruction, just indicate that. Show the control signals for the execution of each of the following instructions. Add any additional control signals to the control signals table **.**

`lwr (load word-register)`

instruction	Meaning	Format					
lwr Rd, Rs (Rt)	Rd = MEM [Rs +Rt]	Op=0	Rs	Rt	Rd	0	0x0e

No modifications are needed. The ALU is used to calculate the address and the destination register should be Rd

Control Signals										
Op	**RegDst**	**RegWr**	**ExtOp**	**ALUSrc**	**MemRd**	**MemWr**	**WBdata**	**ALUOp**	**PCSrc**	
lwr	1	1	X	0	1	0	1	ADD	0	


Branch Target Address
Jump Target = PC[31:28] || Imm26
Next PC Address
ExtOp
Imm16
Ext
+
+1
ALU result
Zero
Instruction Memory
Address
Instruction
PC
Rs
Rt
Rd
RA
RB
RW
BusA
BusB
BusW
Registers
A
L
U
Data Memory
Address
Data_out
Data_in
PCSrc
clk
RegDst
RegWr
func
ALUop
MemRd
MemWr
WBdata
Op
PC Ctrl
ALU Ctrl
Zero
ExtOp
ALUSrc
Main Control

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Control Signals									
Op	**RegDst**	**RegWr**	**ExtOp**	**ALUSrc**	**MemRd**	**MemWr**	**WBdata**	**ALUOp**	**PCSrc**
addi	0	1	1	1	0	0	0	ADD	0
sw	X	0	1	1	0	1	X	ADD	0

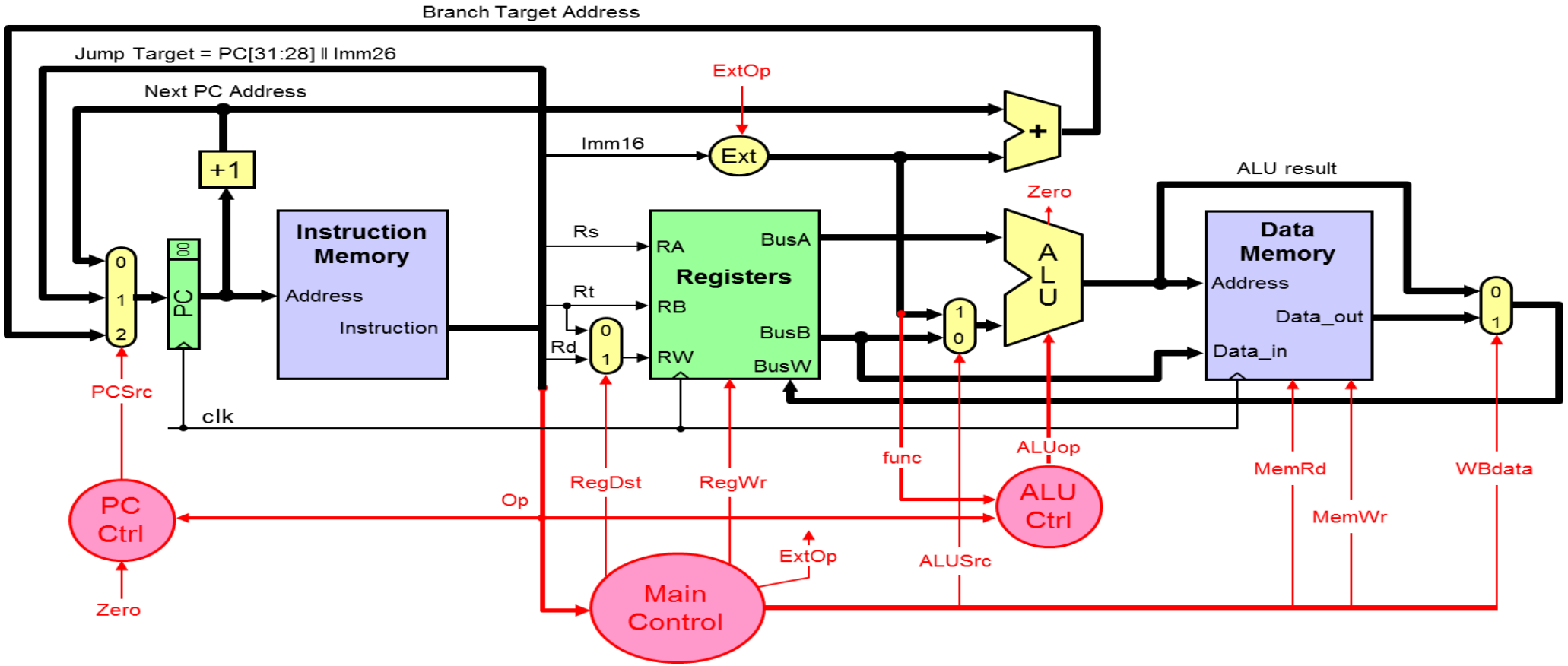
b. (6 points) We want to add the following instructions to the MIPS single-cycle datapath. Made any necessary modifications to the datapath, ALU or PC control block and the control signals needed for the implementation of these instructions. If no modifications to the datapath are required for implementing a given instruction, just indicate that. Show the control signals for the execution of each of the following instructions. Add any additional control signals to the control signals table.

`beqz (branch if equal to zero)`

instruction	Meaning	Format			
beqz Rs, label	If Rs == 0 PC=label	Op=0x01	Rs	0	16-bit offset$_{16}$

No modification needed. The instruction is similar to BEQ where the second register is R0

Control Signals										
Op	**RegDst**	**RegWr**	**ExtOp**	**ALUSrc**	**MemRd**	**MemWr**	**WBdata**	**ALUOp**	**PCSrc**	
beqz	X	0	X	0	0	0	X	SUB	0/2	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Registers
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L
U
Data Memory
Address
Data_out
Data_in
0
1
2
PC
00
PCSrc
clk
RegDst
RegWr
func
ALUop
MemRd
MemWr
WBdata
Op
PC Ctrl
ALU Ctrl
Zero
Main Control
ExtOp
ALUSrc